IN THE CLAIMS:

The status and content of each claim follows.

1. (currently amended) A ~~An electronic~~ circuit in an embedded processing system covering a ~~plurality~~ number of technical applications, [[the]] a number of operative functions of ~~which are~~ the number of technical applications being performed ~~with~~ via a respective ~~plurality~~ number of application-specific Electronic Control Units (ECU), ~~characterized by having~~ the circuit comprising:

a) a ~~plurality~~ number of controller means ~~(**30**A, . . . **30**E)~~ for controlling respective application specific ECUs, ~~comprising~~ each of the controller means comprising ~~a respective one of said~~ a number of application-specific support functions and I/O subsystems; [[,]] and

b) a ~~plurality~~ number of ~~standard~~ processor units ~~(**40**)~~ each having ~~a standard~~ an I/O-interface operatively connecting to a respective one of the controller means ~~(**30**A, . . . **30**E)~~ and supplying [[it]] that controller means with computing power,

~~c)~~ wherein [[a]] at least one of the processor ~~unit~~ units ~~(**40**)~~ and a respective ~~one of said~~ controller means ~~(**30**A, . . . **30**E)~~ are implemented on different chips.

2. (currently amended) The circuit according to claim 1, further ~~having~~ comprising mapping means ~~(**70, 26**)~~ for mapping the I/O subsystems to the processor units, and a General Controller Unit ~~(**12**)~~ operatively coupled ~~thereto~~ to the mapping means and configured to ~~for~~ dynamically ~~switching~~ switch [[a]] at least one of the processor ~~unit~~ units into communication

with ~~(40) to~~ a selected controller means ~~(30A, . . . 30E) under consideration of~~ based on processor timing requirements.

3. (currently amended) The circuit according to ~~the preceding~~ claim 2, ~~having~~ further comprising:

a primary layer ~~(50)~~ comprising basic configuration layout data ~~(54)~~ and ~~a standard~~ an interface means ~~(52)~~ for connecting to ~~said~~ the ~~plurality~~ number of ~~standard processors~~ processor units ~~(40),~~; and

a secondary layer ~~(60)~~ comprising a preprogrammed, ~~"autonomic state"~~ autonomic state switching means ~~(62)~~, a preprogrammed emergency switching means ~~(64),~~ and a port interface means ~~(66)~~ ~~connecting~~ connected to at least one ~~said plurality~~ of ~~application specific~~ the I/O subsystems.

4. (currently amended) The circuit according to ~~the preceding~~ claim 3, further ~~having~~ comprising an additional controller operatively coupled to the General Controller Unit and configured to ~~implementing~~ implement a monitoring function ~~(90,100)~~ for monitoring the operational status of ~~said plurality of standard processing~~ the processor units ~~(40)~~ and the controller means ~~(30A, . . . 30E), and being operatively coupled to said General Controller Unit (12)~~.

5. (currently amended) The circuit according to claim 1, further comprising a database storing instructions on how to handle specific ~~breakdown cases of error state cases~~ errors associated ~~wit~~ with ~~either of said standard processors~~ the number of processor units.

6. (currently amended) The circuit according to claim 1, further comprising a number of emergency ~~controller~~ controllers (**110**, **112**) for continuously storing current global positioning system (GPS) coordinates and ~~dedicated~~ configured to send an emergency signal including ~~said~~ the coordinates[[,]] in case ~~one or more~~ a number of external sensor devices detect an emergency case.

7. (currently amended) An embedded system having an electronic circuit according to ~~one of the preceding claims 1-6~~ claim 1.

8. (new) A method of operating an embedded processing system comprising:

controlling a number of electronic control units with a number of interface expander controllers, wherein said interface expander controllers are disposed on a separate chip from said electronic control units; and

providing computing power to said interface expander controllers with a separate number of processors.

9. (new) The method of claim 8, further comprising selectively providing communication between said interface expander controllers and said processors with a General Controller Unit.

10. (new) The method of claim 8, further comprising disposing said interface expander controllers on a single Application Specific Integrated Circuit.